77. (New) The method of claim 75, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

78. (New) The method of claim 75, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation;

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

79. (New) The method of claim 78, further comprising:

selecting at least one address pathway based on subsequently switching to the burst mode of operation.

80. (New) A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory read operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

81. (New) The method of claim 80, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

82. (New) The method of claim 80, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.